Claims

1. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a circuit pattern over a first main surface of a semiconductor wafer that has a first thickness;

(b) making the semiconductor wafer a second thickness by grinding a second main surface of the semiconductor wafer using a first grinding material which has a fixed abrasive;

(c) making the semiconductor wafer a fourth thickness and forming a second crush layer in the second main surface of the semiconductor wafer by grinding the second main surface of the semiconductor wafer using a third grinding material which has a fixed abrasive a diameter of a particle of which is smaller than the first grinding material; and

(d) individually separating the semiconductor wafer to a chip by dicing the semiconductor wafer;

wherein a particle size of a polish fine powder of the third grinding material is #3000 to #100000.

2. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

a particle size of a polish fine powder of the first grinding material is #100 to #700.

3. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

the particle size of the polish fine powder of the third grinding material is #4000 to #50000.

4. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

the particle size of the polish fine powder of the third grinding material is #5000 to #20000.

5. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

the particle size of the polish fine powder of the third grinding material is #8000 or more than it.

6. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

a thickness of the second crush layer is less than 1 □m.

7. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

a thickness of the second crush layer is less than 0.5 □m.

8. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

a thickness of the second crush layer is less than 0.1 □m.

9. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

the fourth thickness of the semiconductor wafer is less than 100 □m.

10. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

the fourth thickness of the semiconductor wafer is less than 80 □m.

11. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

the fourth thickness of the semiconductor wafer is less than 60 □m.

12. A manufacturing method of a semiconductor integrated circuit device according to claim 1, between the step (b) and the step (c), further comprising the step of:

(e) making the semiconductor wafer a third thickness thinner than the second thickness and thicker than the fourth thickness by grinding the second main surface of the semiconductor wafer using a second grinding material which has a fixed abrasive with a diameter of a particle smaller than the first grinding material and the diameter of the particle larger than the third grinding material.

13. A manufacturing method of a semiconductor integrated circuit device according to claim 12, wherein

a particle size of a polish fine powder of the second grinding material is #1500 to #2000.

14. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a circuit pattern over a first main surface of a semiconductor wafer that has a first thickness;

(b) making the semiconductor wafer a second thickness by grinding a second main surface of the semiconductor wafer using a first grinding material which has a fixed abrasive;

(c) making the semiconductor wafer a third thickness and forming a first crush layer in the second main surface of the semiconductor wafer by grinding the second main surface of the semiconductor wafer using a second grinding material which has a fixed abrasive a diameter of a particle of which is smaller than the first grinding material;

(d) removing the first crush layer of the second main surface of the semiconductor wafer;

(e) forming a third crush layer in the second main surface of the

semiconductor wafer; and

(f) individually separating the semiconductor wafer to a chip by dicing the semiconductor wafer.

15. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

a particle size of a polish fine powder of the first grinding material is #100 to #700.

16. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

a particle size of a polish fine powder of the second grinding material is #1500 to #2000.

17. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

a thickness of the third crush layer is less than 0.5 □m.

18. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

a thickness of the third crush layer is less than 0.3 □m.

19. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

a thickness of the third crush layer is less than 0.1 □m.

20. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

the third thickness of the semiconductor wafer is less than 100 □m.

21. A manufacturing method of a semiconductor integrated circuit

device according to claim 14, wherein

the third thickness of the semiconductor wafer is less than 80 □m.

22. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

the third thickness of the semiconductor wafer is less than 60 □m.

23. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

the step (e) includes the following subordinate step of:

(e1) forming the third crush layer in the second main surface of the semiconductor wafer by injecting an abrasive particle to the second main surface of the semiconductor wafer.

24. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

the step (e) includes the following subordinate step of:

(e1) forming the third crush layer in the second main surface of the semiconductor wafer by impacting an ion produced by plasma electric discharge to the second main surface of the semiconductor wafer.

25. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

the step (e) includes the following subordinate step of:

(e1) forming the third crush layer in the second main surface of the semiconductor wafer by grinding the second main surface of the semiconductor wafer.

26. A manufacturing method of a semiconductor integrated circuit device according to claim 14, wherein

the step (d) includes the following step of:

(d1) making a left-behind first crush layer the third crush layer of the step (e) by removing the first crush layer formed in the second main surface of the semiconductor wafer leaving a part.